IN THE SPECIFICATION:

Please amend the specification as follows:

Please amend paragraph 0030 as follows:

[0030] In FIG. 3, processor 200 may predict (335) a load instruction to be memory renamed to use the same register as a previous instruction, for example, the above store instruction that was written (315) into SAB 232. A load store source index, for example, a SBID, may be computed (340) and a load address, for example, a register address, may also be computed (345) in processor 200 to be the same as the above store instruction (e.g., a source store instruction) and may be used by the load instruction to obtain its data. The memory renamed load instruction may be disambiguated (350) that is a check may be performed to see if the load instruction used the correct data. However, since the store address (e.g., the source store address) is de-allocated from MOB 230 upon completion of the store instruction, disambiguating (350) the memory renamed load instruction may result in the store instruction from which the load instruction was forwarded not being in MOB 230. In accordance with this embodiment of the present invention, disambiguating (350) the memory renamed load instruction may include checking SAB 232 to determine whether the store address is still in SAB 232 and, if the store address is not in SAB 232, determining whether the store address is in TSB 234. If the store address is determined (355) to still be in SAB 232 and/or the store address is determined (360) to be in TSB 234, the memory renamed load instruction may be able to be checked against the store instruction to verify that the memory renaming was correct, if the memory renaming was correct, that is, if the full data of the load instruction should have been provided by the predicted store instruction, the load instruction may be retired (365) and the method may terminate.